

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1.- 13. (canceled).

14. (previously presented): The thin film transistor substrate according to claim 29, wherein at least one of said impurity doping regions formed in a self-aligning manner with respect to said first gate electrode includes an LDD structure.

15. (canceled).

16. (previously presented): The thin film transistor substrate according to claim 29, wherein at least one of impurity doping regions which overlap said second gate electrode includes an LDD structure.

17. - 28. (canceled).

29. (currently amended): A thin film transistor substrate comprising:
an insulating substrate;
a first thin film transistor formed above said insulating substrate, wherein said first thin film transistor comprises a first active layer formed above said insulating substrate, a first gate

insulating film formed on said first active layer, and a first gate electrode formed on said first gate insulating film; and

a second thin film transistor formed above said insulating substrate, wherein said second thin film transistor comprises a second active layer formed above said insulating substrate, a second gate insulating film formed on said second active layer, and a second gate electrode formed on said second gate insulating film,

wherein said second gate insulating film comprises said first gate insulating film and a gate cover film formed above said first gate insulating film,

wherein said second active layer has at least two impurity doping regions which overlap said second gate electrode,

wherein said first active layer has at least two impurity doping regions formed in a self-aligning manner with respect to said first gate electrode,

wherein said second thin film transistor further comprises a third gate electrode, wherein a gate length of said third gate electrode is shorter than a gate length of said second gate electrode, wherein said third gate electrode is formed between said second active layer and said second gate electrode and on the first gate insulating film,

wherein said impurity doping regions formed in a self-aligning manner are formed so as to overlap said first gate electrode by 0.1 μm or less, and

wherein said second active layer comprises a first channel region disposed directly below said second gate electrode, a second channel region disposed directly below said third gate electrode and an impurity doping region is-disposed between said first and second channel

regions such that a portion of said impurity doping region is not directly below either said second gate electrode or said third gate electrode.

30. (previously presented): The thin film transistor substrate according to claim 29 wherein said impurity doping regions which overlap said second gate electrode are formed so as to overlap said second gate electrode by 2.0 μm or less.

31. (previously presented): The thin film transistor substrate according to claim 29 wherein said third gate electrode comprises a two-layer structure including a semiconductor layer and a metal or a metal silicide layer.

32. (previously presented): The thin film transistor substrate according to claim 29, wherein said second gate electrode comprises a semiconductor layer.

33. (previously presented): The thin film transistor substrate according to claim 29, wherein said third gate electrode is formed of the same material as said first gate electrode, and

wherein said third gate electrode has the same thickness as said first gate electrode.

34. (previously presented): The thin film transistor substrate according to claim 29, wherein said first gate electrode, said second gate electrode and said third gate electrode are formed under wires which connect to said impurity doping regions.

35. (previously presented): The thin film transistor substrate according to claim 29, wherein the impurity doping region existing between the second gate electrode and the third gate electrode is an LDD region.

36. (new): The thin film transistor substrate according to claim 29, wherein said first channel region, said second channel region and said impurity doping region are configured in a plane configuration.